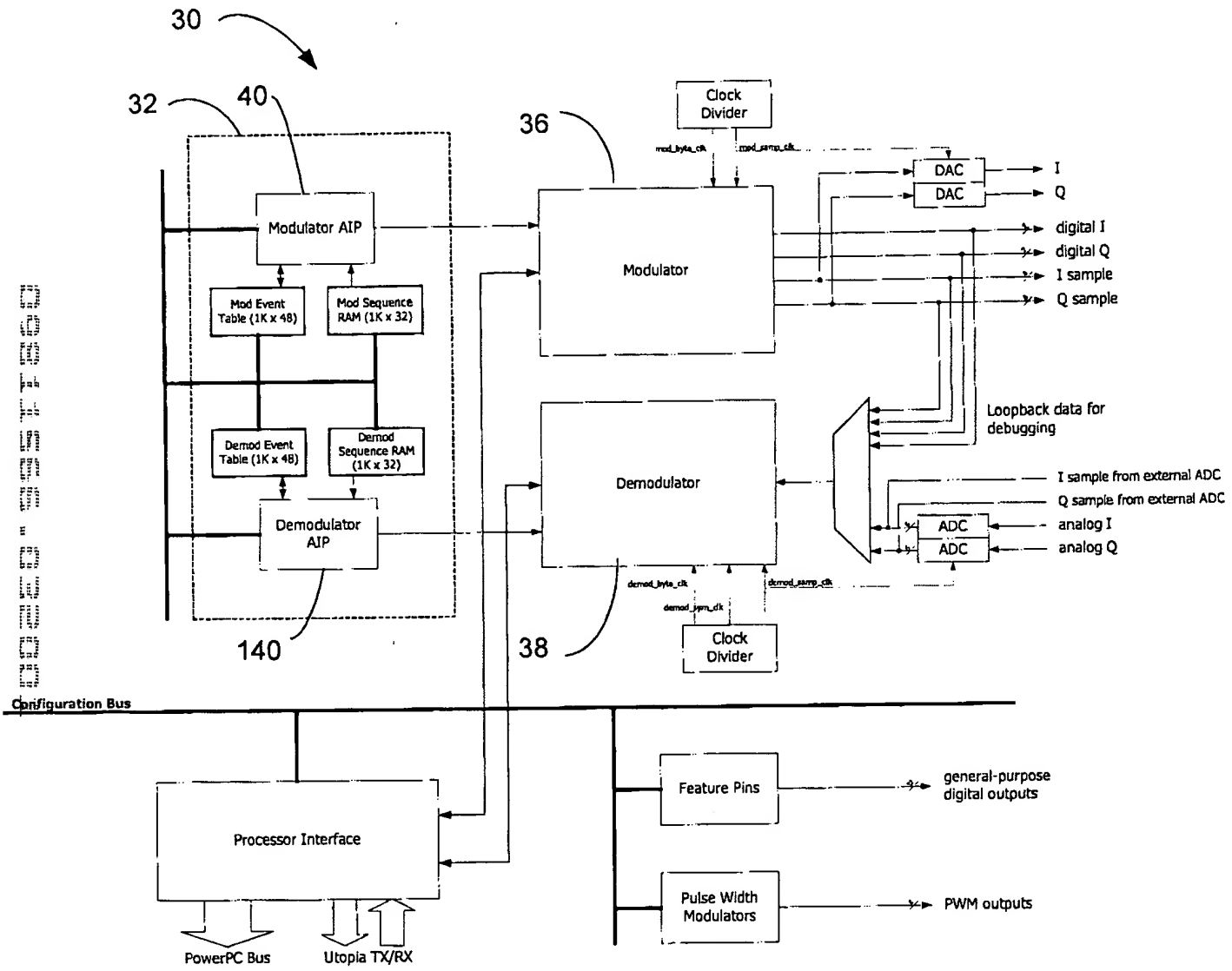
30
32
40
36
Clock Divider
Modulator AIP
Mod Event Table (1K x 48)
Mod Sequence RAM (1K x 32)
Modulator
DAC
DAC
I
Q
digital I
digital Q
I sample
Q sample
Demod Event Table (1K x 48)
Demod Sequence RAM (1K x 32)
Demodulator
Loopback data for debugging
I sample from external ADC
Q sample from external ADC
ADC
ADC
analog I
analog Q
Demodulator AIP
140
38
Clock Divider
Configuration Bus
Feature Pins
general-purpose digital outputs
Processor Interface
Pulse Width Modulators
PWM outputs
PowerPC Bus
Utopia TX/RX

Figure 1

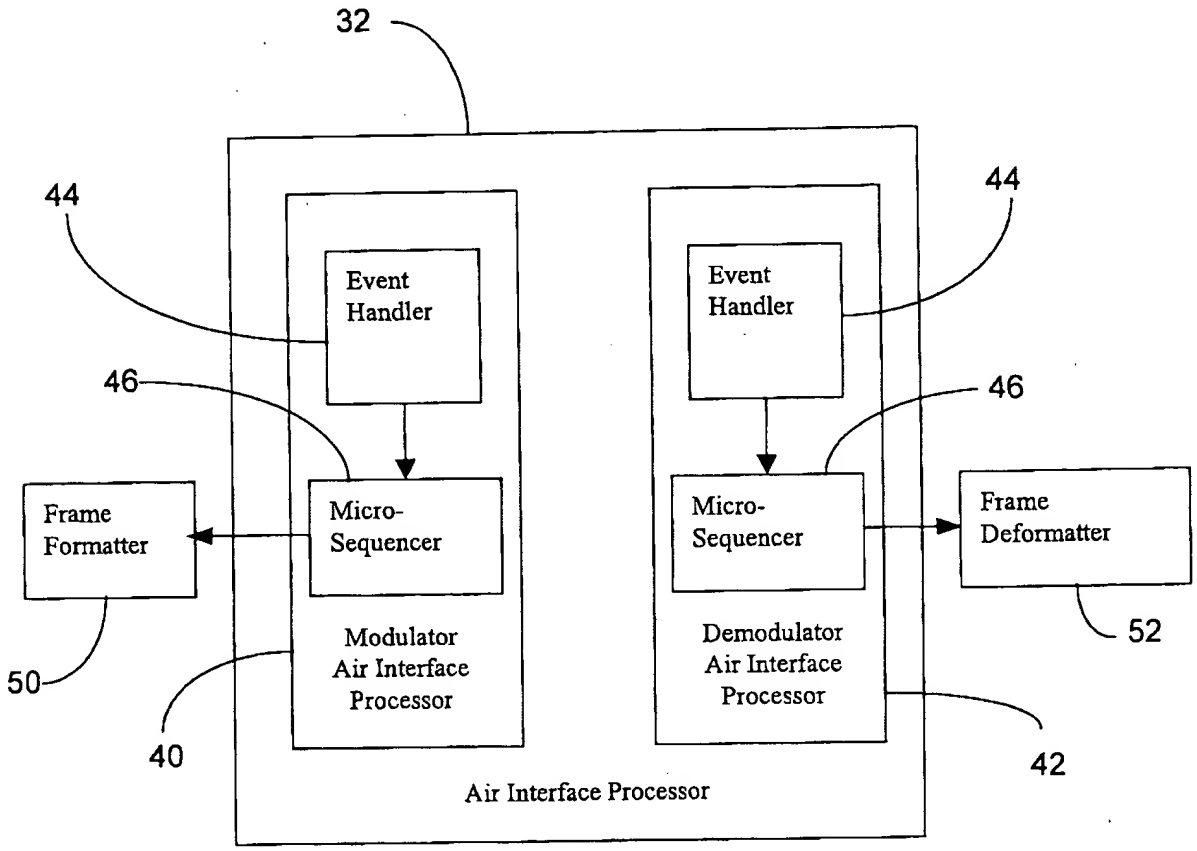
32
44
Event Handler
46
Frame Formatter
Micro-Sequencer
Modulator Air Interface Processor
50
40
44
Event Handler
46
Micro-Sequencer
Frame Deformatter
52
Demodulator Air Interface Processor
42
Air Interface Processor

Figure 2

Instruction	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type 1	0	0	ALU opcode					S	W	Rd				Rn				operand 2													branch code											pass address										fail address										
Type 2	0	1	0	0	Rhi					-				Rlo	32-bit data																																					
Type 3	0	1	0	1	Rhi					Imm_lo					32-bit data																																					
Type 4	0	1	1	0	Rhi					-				Rlo	-																																			Rd				
Type 5	0	1	1	1	Rhi					Imm_lo					-																																			Rd				
Type 6	1	T	D	Q				0	Microsequencer address						trigger time																																									
Type 7	1	-						0	1	-	burst info																																											
Type 8	1	-	A	1	1	-	mask																																													

Instruction Type 1: ALU Operations
Instruction Type 2: Write register
Instruction Type 3: Write register immediate
Instruction Type 4: Read register
Instruction Type 5: Read register immediate
Instruction Type 6: Trigger
Instruction Type 7: BURST
Instruction Type 8: WAIT
[A='0' → until any of (R12 and mask) bits are set]
[A='1' → until all of (R12 and mask) bits are set]

Figure 3: Event Handler Instruction Set Summary

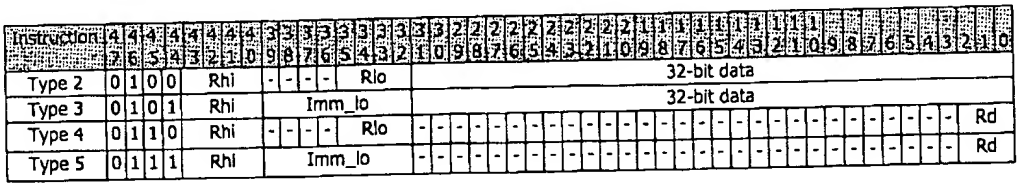

Figure 4: Register Access Instructions

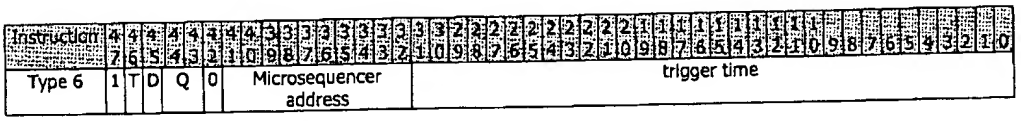

Figure 5: Data Scheduling Instructions

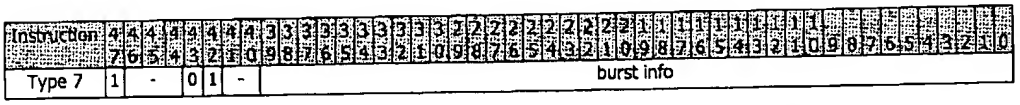

Figure 6: Burst Descriptor Instruction

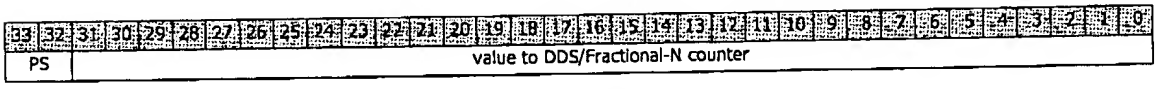

Figure 7: Modulator Burst Info Field Format

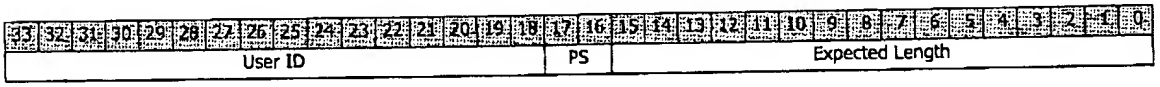

Figure 8: Demodulator Burst Info Field Format

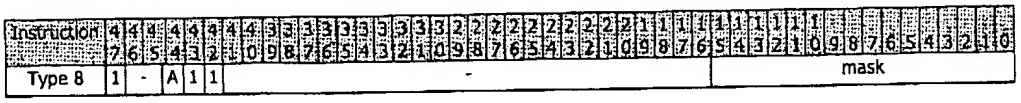

Figure 9: Processor Wait Instruction

opcode	name	Description
00000	JZ	Jump to Zero
00001	CJS	Conditional Jump to Subroutine
00010	JMAP	Jump Map
00011	CJP	Conditional Jump Pipeline
00100	PUSH	Push/Conditional Load Counter
00101	JSRP	Conditional Jump to Subroutine
00110	CJV	Conditional Jump Vector
00111	JRP	Conditional Jump
01000	RFCT	Repeat Loop Counter Not Equal to Zero
01001	RPCT	Repeat Pipeline Counter Not Equal to Zero
01010	CRTN	Conditional Return
01011	CJPP	Conditional Jump Pipeline and Pop
01100	LDCT	Load Counter and Continue
01101	LOOP	Test End of Loop
01110	CONT	Continue
01111	TWB	Three Way Branch
10000	FORK	Multiway Branch
others		reserved

Figure 10: Microsequencer Instruction Set

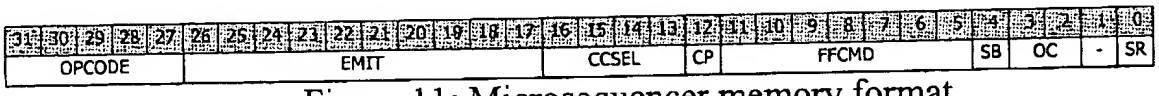

Figure 11: Microsequencer memory format

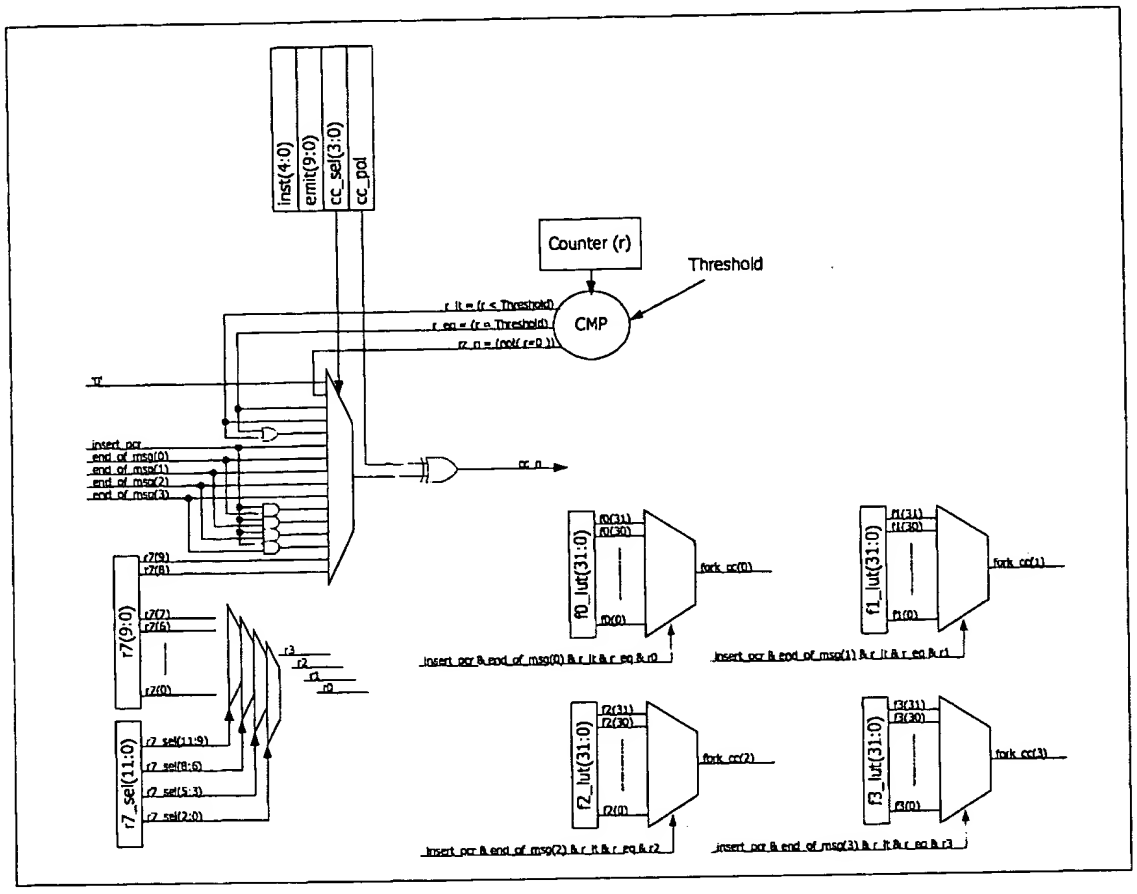

Figure 12: Configuration of condition codes and fork

1	x	x	1	x	Match	
0	0	0	0	0	0	0
0	0	0	0	1	0	
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	0	0
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	0	
0	1	0	0	0	0	0
0	1	0	0	1	0	
0	1	0	1	0	0	
0	1	0	1	1	0	
0	1	1	0	0	0	0
0	1	1	0	1	0	
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	0	C
1	0	0	0	1	0	
1	0	0	1	0	1	
1	0	0	1	1	1	
1	0	1	0	0	0	C
1	0	1	0	1	0	
1	0	1	1	0	1	
1	0	1	1	1	1	
1	1	0	0	0	0	C
1	1	0	0	1	0	
1	1	0	1	0	1	
1	1	0	1	1	1	
1	1	1	0	0	0	C
1	1	1	0	1	0	
1	1	1	1	0	1	
1	1	1	1	1	1	

Figure 13

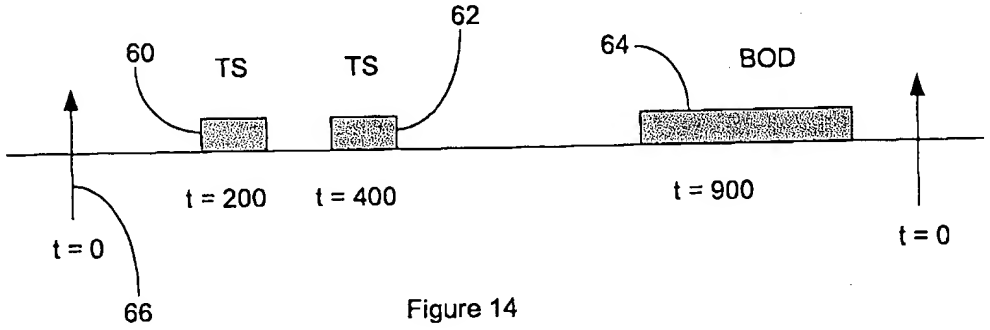

Figure 14

Event Handler 44

Time	Sequence
T=200	TS
T=400	TS
T=600	BOD

Figure 15

Microsequencer 46

Sequence	Actions
TS	send header send 1 ATM cell add RS encoding
BOD	send header send 3 ATM cells add RS encoding

68

70

Figure 16

Terminal Modulator Block Diagram

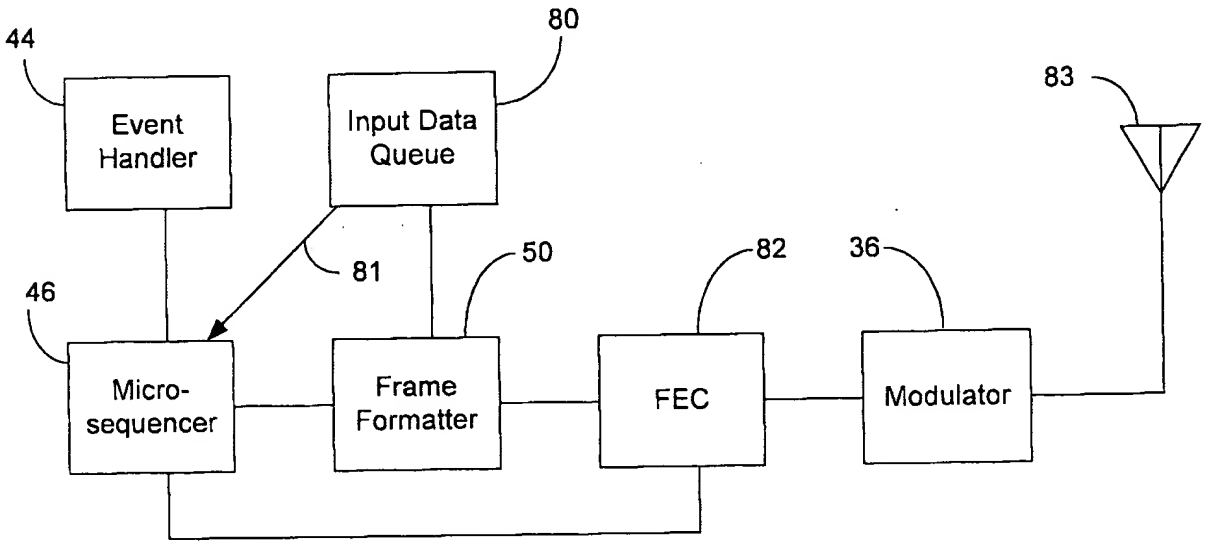

Fig 17

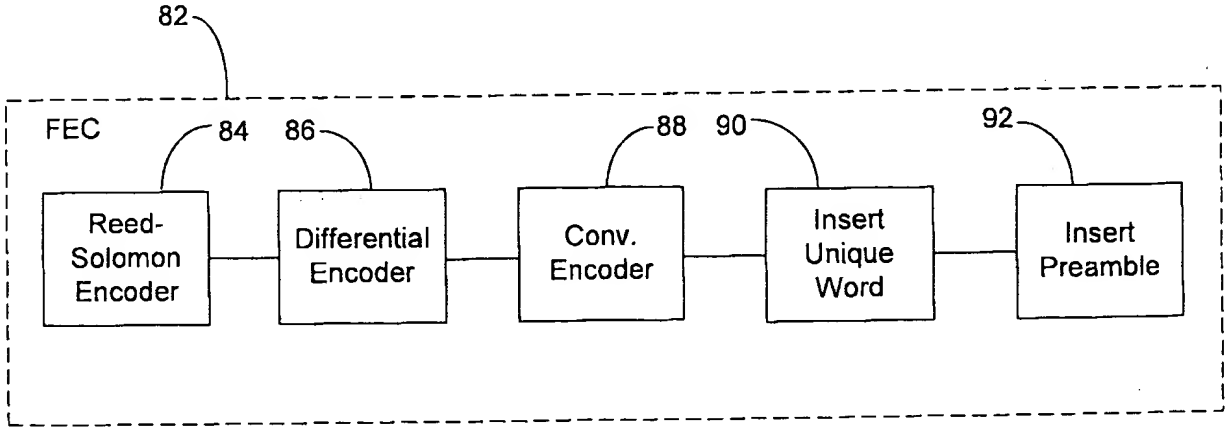

Fig 18

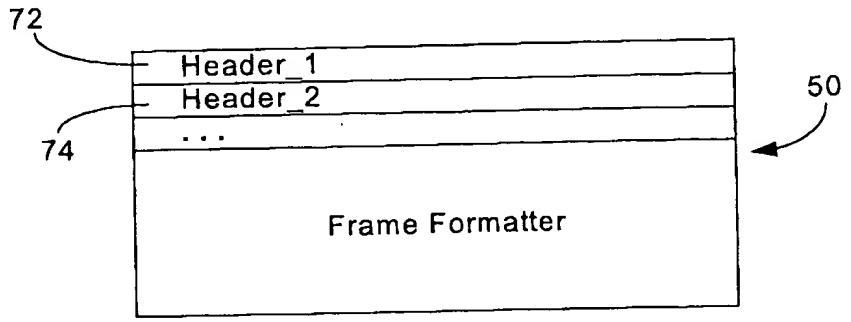

Figure 19

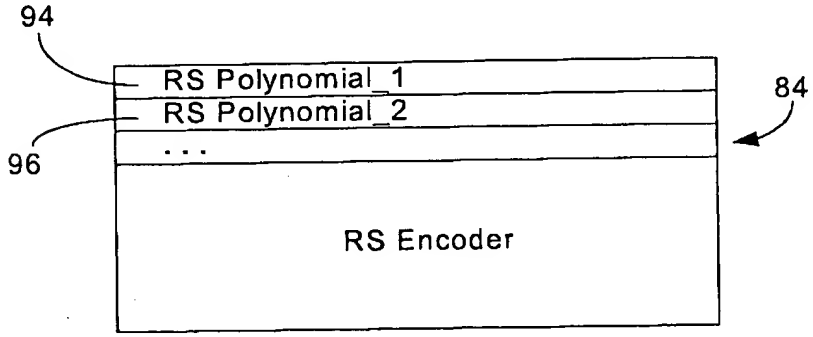

Figure 20

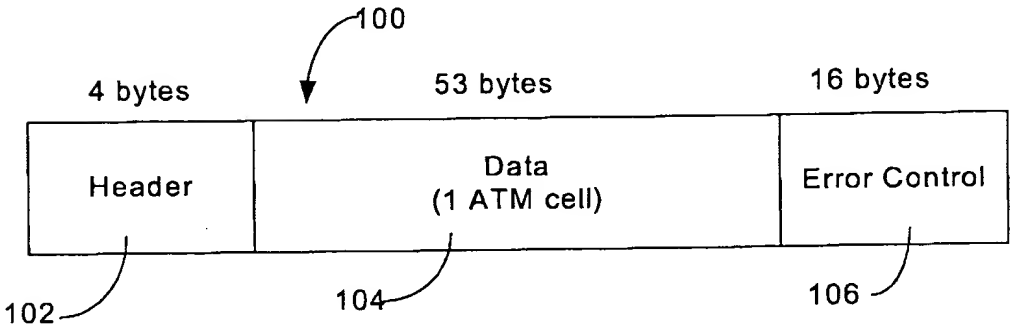

Figure 21

Terminal Demodulator Block Diagram

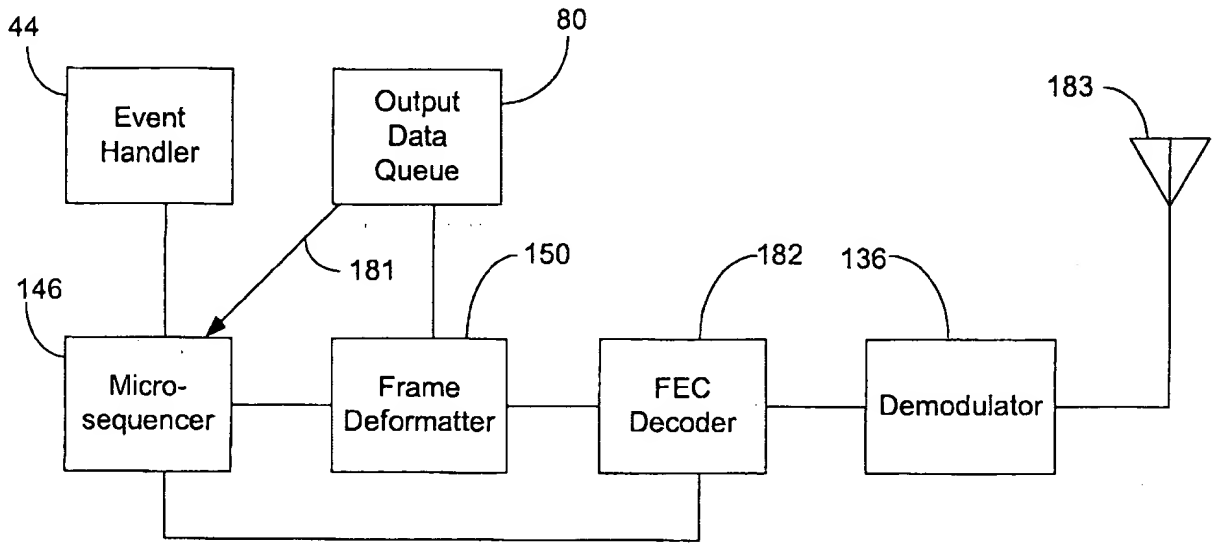

Fig 22

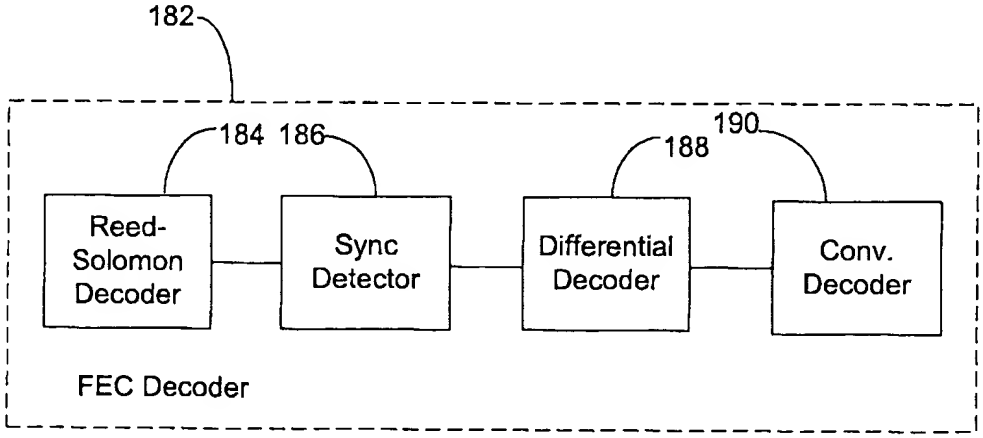

Fig 23